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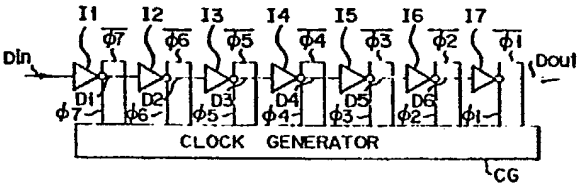
(54) **Data delay/memory circuit.**

(57) A data delay/memory circuit includes clock-controlled data latch circuits formed with cascade-connected clocked inverters (I1-I7). The data delay/memory circuit also includes a clock generator (CG) for supplying the clocked inverters (I1-I7) with clock signals (ϕ1-ϕ7, $\overline{\phi 1}$-$\overline{\phi 7}$). These clock signals (ϕ1-ϕ7, $\overline{\phi 1}$-$\overline{\phi 7}$) have individual clocking phases and are sequentially generated such that the clocking phase for a final stage (I7) of the data latch circuits is ahead of that for an initial stage (I1) thereof.

FIG. 1



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Data delay/memory circuit

The present invention relates to a data delay/memory circuit which memorizes input data for a given period of time and, thereafter, outputs the memorized data.

Signal processing for temporary memorizing and delaying a digital signal is conventionally effected in a digital 1H memory which delays by one horizontal period of time (1H) a horizontal video signal of a digital TV, in a digital filter, in a deinterleave circuit of a compact disc player, or in the like.

In a prior art data delay/memory circuit used for the above exemplified applications, a plurality of cascade-connected one-bit shift registers are conventionally adapted. The number of the cascade connections depends on the circuit design. Each of these one-bit shift registers comprises a pair of clocked inverters for latching input data. One clocked inverter of the pair operates in synchronism with a clock signal, while the other clocked inverter operates in synchronism with an antiphase clock signal. According to such a prior art data delay/memory circuit, a one shift register is inevitably provided for storing each one bit data. Consequently, the necessary number of the data latching, clocked inverters has to be twice the number of the one bit shift registers. If a 1H memory of a digital TV

Claims:

1. A data delay/memory circuit comprising: (Fig. 1)

a data shift circuit formed of a plurality of clock-controlled data latch circuits (I1-I7) which are cascade-connected; and

means (CG) for supplying said plural data latch circuits (I1-I7) with clock signals (φ1-φ7) having individual clocking phases and being sequentially generated such that the clocking phase (φ1) for a final stage (I7) of said data latch circuits is ahead of that (φ7) for an initial stage (I1) of said data latch circuits.

2. A data delay/memory circuit according to claim 1, characterized in that each of said data latch circuits is of a dynamic type.

3. A data delay/memory circuit according to claim 2, characterized in that said dynamic data latch circuits include clocked inverters.

4. A data delay/memory circuit according to claim 1, characterized in that said supplying means (CG) is provided with wirings (W10-W23) for feeding said clock signals (φ1-φ7) which geometrically cross the data transfer direction of said cascade-connected plural data latch circuits.

5. A data delay/memory circuit comprising: (Figs. 3, 5)

a plurality of data delay/memory circuits (DMC1-DMC6) each being formed of a plurality of clock-controlled and cascade-connected data latch circuits (I1A-I7F):

means (CG) for supplying said plural data latch circuits (I1A-I7F) with clock signals (φ1-φ7) having individual clocking phases and being sequentially generated such that the clocking phase (φ1) for a final stage (I7) of each of said data latch circuits is ahead

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FIG. 1

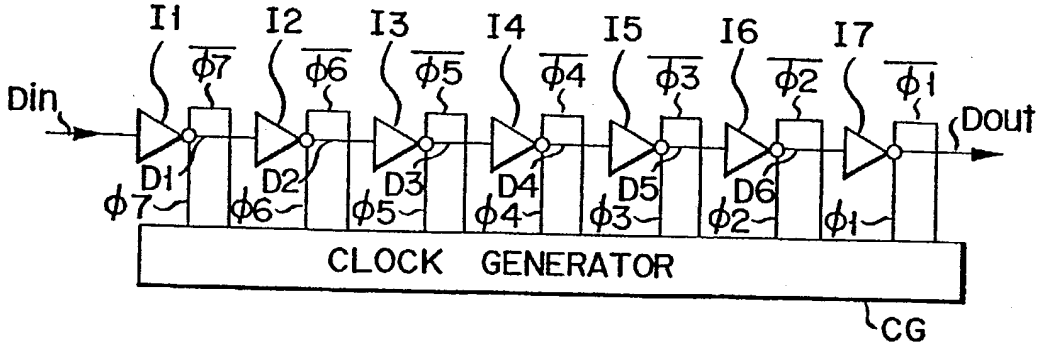

FIG. 5